Improved Post-etch Via Clean With Fluoride-based Semi-Aqueous Chemistry Using an Intermediate Rinse

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INTRODUCTION:

The hydroxylamine-based products are regarded as the industry standard in residue removal. Standard amine-based and hydroxylamine-based chemistries have shown good cleaning performance, but need high temperatures and 15-45 min process times.

The introduction of semi-aqueous cleaning (SAC) chemistries for post metal etch and post via etch cleaning is another option. Semi-aqueous fluoride chemistries are composed of organic solvents, water, low concentrations of fluoride species and certain “buffering” agents to control the fluoride chemical activity. Most of the semi-aqueous fluoride chemistries can be used at near ambient temperatures (23 to 30 C) with shorter process times, are rinseable in water and can reduce water-rinse volumes. (1)

The typical wet chemical cleaning process for post etch residue (PER) removal involves two critical steps. The first step involves removing the etch residue with an active chemistry. The second step involves the rinse process, whether the wafer goes directly into DI water or involves an intermediate rinse before the water step.

INTERMEDIATE RINSE PROCESS:

This paper studies an improved post-etch via cleaning process using fluoride-based semi-aqueous chemistry in a multi-position spray-processing tool. The cleaning mechanism for traditional amine-based and hydroxylamine-based chemistries operates by simply dissolving the post etch residues (PER) from the outer surface into the structure and leaving a temporary absorbed layer of nitrogen- or corrosion inhibitor species on the cleaned surfaces. (2)

Semi-aqueous fluoride chemistries clean IC metal structure by a diffusional process. As the chemistries diffuse into the PER the “polymeric” inorganic/organic residues are converted into smaller subspecies. Because of the low water content in the chemistry only a small portion of these “subspecies” are dissolved. Most of this converted material remains in place until the DI water rinse step.

The improved via clean process takes advantage of the diffusional activity. The process involves a short (90 second) dispense of the semi-aqueous chemistry, followed by a short (30 second) rinse with DI water. The intermediate DI rinse is followed by a second short (90second) semi-aqueous chemical dispense. The process then finishes with a rinse and dry. The chemicals are dispensed at a high rate of flow while the wafers are at a high spin rate. The intermediate DI rinse is also dispensed at a high spin rate.

The final rinse sequence is also critical. It starts after the second semi-aqueous chemical dispense with a high spin speed and a high DI flow rate. A "ramped" rinsing sequence and then the wafer dry step follows this. All rinsing is kept as short as possible to minimize the time metal is exposed to DI water.

Figure 1 shows the initial condition of the via wafer after etch and ash processing. The results of the improved process (Figure 2) can be contrasted with the results of a process in which the semi-aqueous chemical was dispensed continuously for 5 minutes and then rinsed and dried. (Figure 3) While most of the obvious residues have been removed, there is still substantial sidewall residue remaining in the via. The continuous dispense process uses 66% more chemical, yet does not remove all of the post etch residue. There is no obvious corrosion damage to the underlying metal in either process. Via dimensional gain, due to interlayer dielectric etch, is also minimal.

Finally, this paper will present more data showing the effectiveness of the intermediate rinsing process sequence and offer theories as to why it works better than a simple single dispense process.

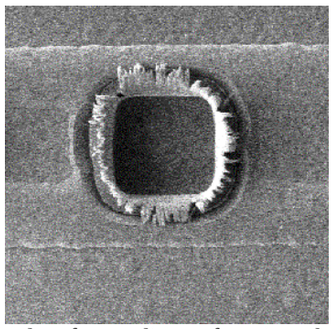

Figure 1: Initial wafer condition after via etch and photo-resist ash.

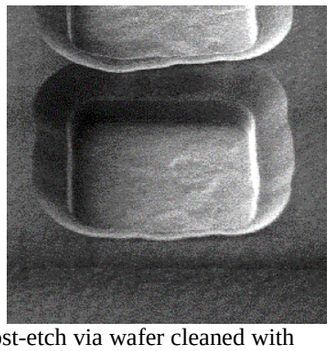

Figure 2: Post-etch via wafer cleaned with dispense/rinse/dispense process.

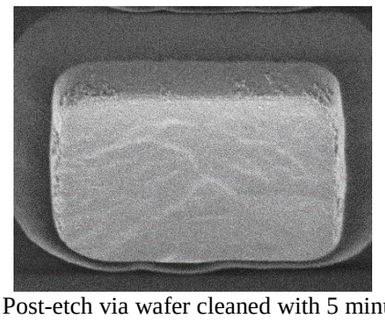

Figure 3: Post-etch via wafer cleaned with 5 minute dispense. Sidewall residue remains.

[1] S.Kirk, R.Small, UCPSS, Solid State Phenomena Vols. 76-77 pp.307-310, (2001)

[2] C.Helms, Contamination Control and Defect Reduction in Semiconductor Manufacturing III, p.222, (1994)